

ABSTRACT OF THE DISCLOSURE

A level shift circuit whereby a voltage shift amount is large, operation speed is fast, and the power consumption is low. A p-type first transistor is connected between the power supply line and the first node, a p-type second transistor is connected between the power supply line and the second node, and an n-type third transistor is connected between the ground line and the first node, and an n-type fourth transistor is connected between the ground line and the second node. The gate of the first transistor is connected to the second node, and the gate of the second transistor is connected to the first node. An input signal is supplied to the gate of the third transistor and an inverted value of the input signal is supplied to the gate of the fourth transistor. Additionally, this level shift circuit has a plurality of control transistors. The control transistor switches the ratio of the inflow current and emission current of the first node or the second node according to the control signal. The operation speed increases if this ratio is set high, and the voltage shift amount increases if this ratio is set low.